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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,237	09/27/2002	Tsai-Sheng Chiu	IEIP0004USA	9439

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NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

DALEY, CHRISTOPHER ANTHONY

ART UNIT	PAPER NUMBER
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2111

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/065,237

Applicant(s)

CHIU, TSAI-SHENG

Examiner

Christopher A. Daley

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 September 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1 – 13 are pending.

Response to Arguments

Applicant's arguments, filed March 17, 2005, with respect to the rejection(s) of claim(s) 1 - 13 under Moore and Shay have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Yen (US5852725).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 - 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Yen (US5852725) as applied to claim 1 above, and further in view of Horan et al (US5892964) herein after Horan.

2. As to claim 1, Yen discloses a central processing unit (CPU) interface card having an accelerated graphic port (AGP) for adapting to a computer backplane to form a computer system, the CPU interface card comprising:

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a plurality of extended industry standard architecture (EISA) contact pads corresponding to an EISA bus for electrically connecting to the computer backplane, the EISA contact pads transferring data between the computer backplane and CPU card according to the EISA bus; (Yen teaches of a CPU card of figure 3 with a plurality of EISA contact pads 31 and 32 for transferring data between the backplane and the CPU card)

Yen does not explicitly disclose a plurality of AGP contact pads interlaced with the EISA contact pads in compliance with the standard configuration of the EISA contact pads to constitute an AGP bus thereby transferring image data between the CPU interface card and the computer backplane. (However, Horan teaches in figure 4 of a slot that would use the ISA bus to power the AGP slot in a board that interlaces PCI and ISA, COL13, lines 35 – 57. It would have been obvious to combine the teachings of Horan into Yen to support legacy boards that combine AGP and PCI slots, COL. 5, lines 5 – 10).

3. As to claims 2, 3, 6, and 7, Yen discloses the CPU interface card as described in claim 1 wherein the AGP contact pads of the CPU interface card are inserted into and then electrically connected with an EISA expansion slot of the computer backplane for image data transmission. (Yen teaches in figure 4 of connecting being made between the contacts on the CPU card of figure 3 and connectors 31 for the ISA bus and the requisite slot of the single CPU board, COL. 3, lines 30 - 35).

4. As to claims 4 and 11, Yen discloses the CPU interface card as described in claim 1 wherein the AGP contact pads of the CPU interface card are interlaced with the EISA contact pads to increase disposition variation of the AGP contact pads and the EISA contact pads on the CPU interface for space saving. (Yen teaches of a CPU interface card where the contact pads of the AGP and EISA are interlaced for space savings, COL. 2, lines 22 - 24).

5. As to claim 5, Yen discloses a CPU interface card having an AGP for adapting to a computer backplane to form a computer system, the CPU interface card comprising at least:

a plurality of peripheral component interconnect (PCI) contact pads corresponding to a PCI bus which serves data transmissions between the computer backplane and the CPU interface card when the PCI contact pads are electrically connected to the computer backplane; (Yen teaches of a CPU card in figure 3 that comprises of contacts to support the PCI bus system, COL. 2, lines 13 – 18).

Yen discloses a plurality of AGP contact pads disposed apart from the PCI contact pads in a predetermined distance to constitute an AGP bus thereby transferring image data between the computer backplane and the CPU interface card when the AGP contact pad are electrically connected to the computer backplane. (Yen teaches in Figure 3 of the interlacing of tow EISA busses with one used to transmit AGP signal, and the other transmit PCI signals, COL. 2, lines 9 - 14).

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6. As to claim 8, Yen discloses a CPU interface card having an AGP for adapting to a computer backplane to form a computer system, the CPU interface card comprising: a plurality of PCI contact pads corresponding to a PCI bus which serves data transmission between the computer backplane and the CPU interface card when the PCI contact pads electrically connected to the computer backplane; (Yen teaches of a CPU card in figure 3 that comprises of contacts to support the PCI bus system, COL. 2, lines 13 – 18).

Yen teaches a plurality of EISA contact pads disposed apart from the PCI contact pads in a predetermined distance to constitute a EISA bus which serves data transmission between the computer backplane and the CPU interface card when the EISA contact pads are electrically connected to the computer backplane; (Yen teaches in Figure 3 of the interlacing of tow EISA busses with one used to transmit AGP signal, and the other transmit PCI signals, COL. 2, lines 9 – 14)

and Yen teaches a plurality of AGP contact pads interlaced with the EISA contact pads, in compliance with the standard configuration of the EISA contact pads to constitute an AGP bus which serves data transmission between the computer backplane and the CPU interface card when the AGP contact pads are electrically connected to the computer backplane. (Yen teaches of two EISA compliant busses comprising interlaced groups of connectors. Yen teaches that the first set of EISA contacts are used for ISA signals and connectors, and it is well known in the art of computer backplane that the AGP signals uses the ISA connectors, COL. 2, lines 30 – 35)

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As to claims 9 and 10, Yen discloses the CPU interface card as described in claim 8 wherein the AGP and EISA contact pads of the CPU interface card are inserted into and then electrically connected to an EISA expansion slot disposed on the computer backplane for image data transmission. (Yen teaches in figure 4 of connection being made between the contacts on the CPU card of figure 3 and connectors 31 for the ISA bus (which is the AGP bus) for image transmission) and the requisite slot of the single CPU board, COL. 3, lines 30 – 35).

7. As to claim 12, Yen discloses the CPU interface card of claim 8 wherein the PCI contact pads of the CPU interface card are inserted into and then electrically connected to a PCI expansion slot for data transmission. (Yen teaches in figure 4 of connection being made between the PCI contact pads of the CPU board of figure 3 and the expansion slot of figure 4, COL. 3, lines 18 - 22).

8. As to claim 13, Yen discloses The CPU interface card of claim 8 wherein the PCI contact pads and the EISA contact pads are disposed in alignment on the CPU interface card for proper respective insertion into the PCI expansion slot and the EISA expansion slot. (Yen teaches that the contact pads for both PCI and EISA are appropriately aligned to proper insertion in the respective expansion slots, Col3, lines 17 - 22).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CAD
5/05/05



TIM VO
PRIMARY EXAMINER